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Built-In Coarse Gain Calibration, Resolution Two-Step TDC CMOS by Pulse-Shrinking Fine Stage

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Abstract: *This article proposes a computerized converter (TDC) solution that can meet a broad range of knowledge and fine-time goals at the same time. The proposed TDC utilizes a beat contracting (PS) plot for a precise target and two-advance (TS) engineering for a larger range in the second phase. The suggested PS TDC solves the undesired non-uniform contracting rate issue that plagues conventional PS TDCs by using an assumed counterbalance beat and a balance beat width detecting method. Due to sign spread and extension fraud between coarse and fine phases, the proposed TS architecture achieves nonlinearity with a few methods, resulting in an inferred coarse increase adjustment mechanism. The replication findings in a 0.18-m normal CMOS innovation show 2.0-ps targets and 16-piece go connected to 130-ns input time interim of 0.08-mm2 area in a TDC modification. With an 18.0 maws 1.8-V supply, it has a single-shot accuracy of 1.44 ps and operates at 3.3 MS/s.*

Keywords*: Built-in coordination includes beat contracting (PS), transition time-to-advanced, and two-stage transition time-to-advanced (TS)*

I. Introduction

Time resolution is increasingly superior than voltage resolution because to recent advances in Cmos manufacturing scale, high-speed transistors, and reduced supply voltage [1], [2]. The usage of a time-to-digital converter has lately benefitted ADPLLs, space scientific software, jitter computations, and other applications (TDC). It's also utilized in estimates of high-precision flight times, which are becoming more common as TDC efficiency increases.

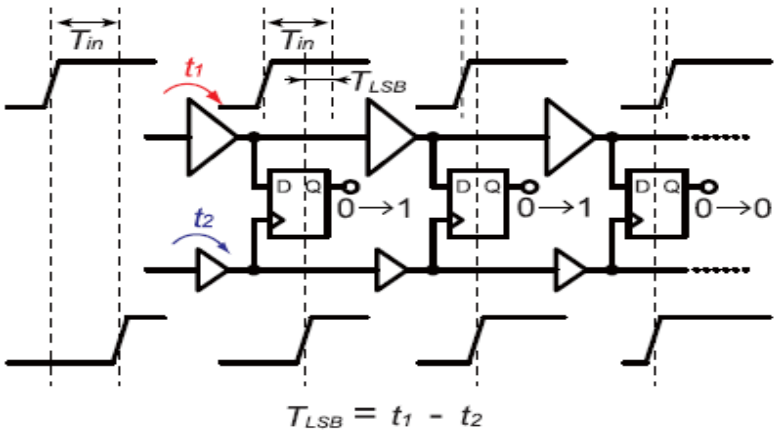


Figure no 1: Simplified schematic of a typical Venire TDC

The laser range finder [3] and mass spectrometry [4] are two examples of testing applications. For fluorescence lifetime, it is often employed in imaging systems [5]. In these applications, which are the study's

primary target applications, fine temporal accuracy and a wide dynamic range are needed [6]. The TDC calculates the total measurement efficiency, thus a few PHS time resolutions with minimal jitter at multiple MS/s samplingrates are always required. In terms of fine resolution, many time conversion methods with sub-gate-delay resolution have been suggested. The Venire TDC is widely used [6]-[9] because to the flexibility of its design concept. A traditional Venire TDC requires two independent delay lines, which are usually linked as ring delay lines to reduce space, as illustrated in Fig. 1. Because two lines have different delay stages, such as t1 and t2, the initial time period Tin decreases as the lower delay line's change catches up with the higher delay line's change (t2 t1). By changing the delay distinction TLSB = t1-t2, we may achieve precise time resolution. This design, on the other hand, is made up of two independent delay lines with a mismatch built in.

The pulse-shrinking (PS) TDC, which is also a kind of Venire TDC, is illustrated in Fig. 2 [10], [11], and uses the delay gap between rising and lowering buffer transitions rather than two distinct delay lines.

The buffer is designed to produce variable rise and fall delays, such as trend t f, when the input pulse width decreases TLSB = tryt f as it propagates through each buffer level (t f try). As opposed to Venire's TDCs,

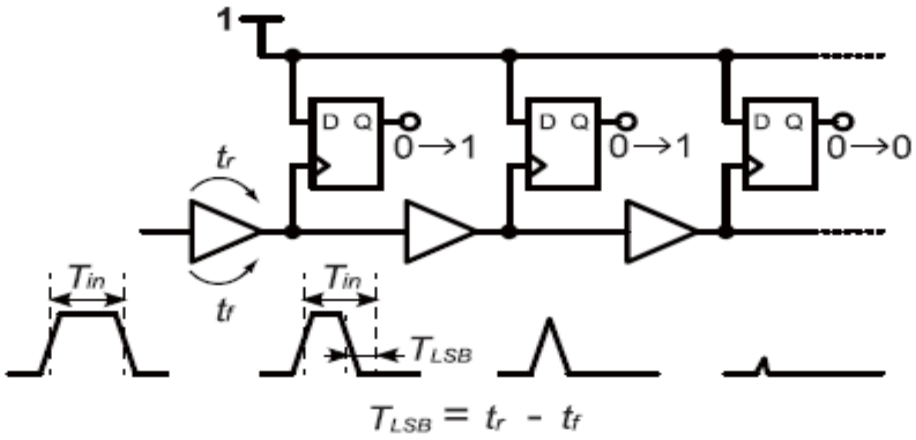


Figure no 2: Simplified schematic of a typical PS TDC

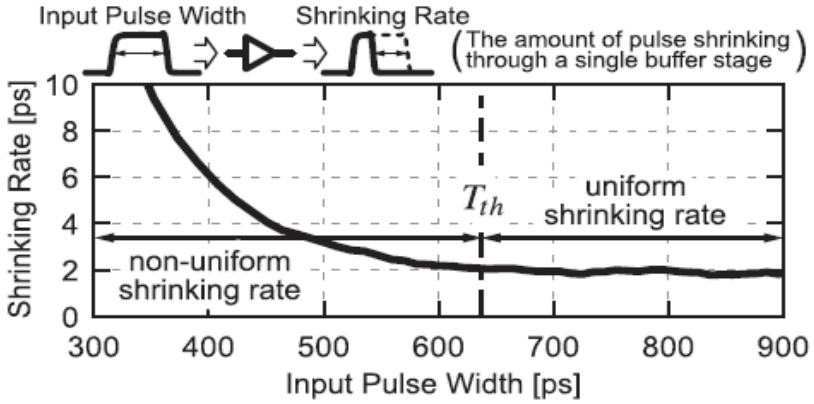


Figure no 3: Simulated PS rate versus input pulse width

Until recently, TDCs have been built with precision time resolution in mind. It may, however, become unattractive over a broad dynamic range. Venire TDCs with an N-bit resolution and a 2N dynamic spectrum, for example, have 2N delay elements and a 2N dynamic spectrum. The dynamic spectrum is halved when the temporal resolution is cut in half. The TDC needs additional 2N delay components to retain the same dynamic range, which increases area occupancy, lowers conversion rate, and increases jitter accumulation as N rises. One of the major ideas for enhancing dynamic range while avoiding a rise is a looping TDC design [13]. The number of cycles the loop's start signal rotates before the stop signal catches up is determined by a loop counter. Using the counter

performance and the thermometer code given by the DFFs, the total conversion result may be determined. The input spectrum may be obtained in the best-case scenario.

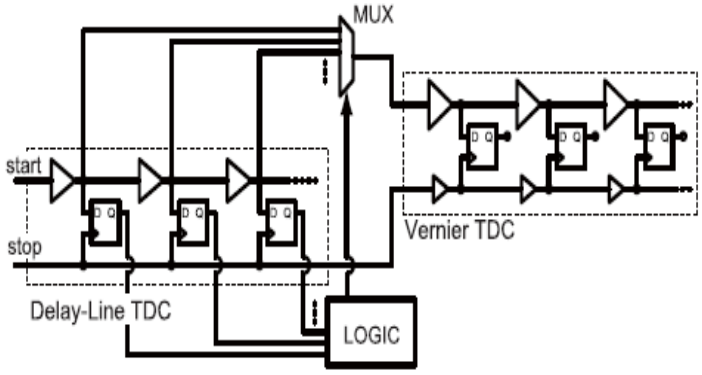


Figure no 4: Schematic of a typical TS TDC [14], [15]

TDCs have been designed with precise time resolution in mind until recently. However, over a wide dynamic range, it may become unappealing. Venire TDCs, for example, have 2N delay elements and a 2N dynamic spectrum when they have an N-bit resolution and a 2N dynamic spectrum. When the temporal resolution is reduced in half, the dynamic spectrum is halved. To maintain the same dynamic range, the TDC requires extra 2N delay components, which increases area occupancy, decreases conversion rate, and increases jitter buildup as N grows. A looping TDC design [13] is one of the most popular ways to increase dynamic range while avoiding a rise. A loop counter determines how many cycles the loop's start signal spins before the stop signal catches up. The overall conversion result may be calculated using the counter performance and the thermometer code provided by the DFFs. In the best-case situation, the input spectrum may be acquired.

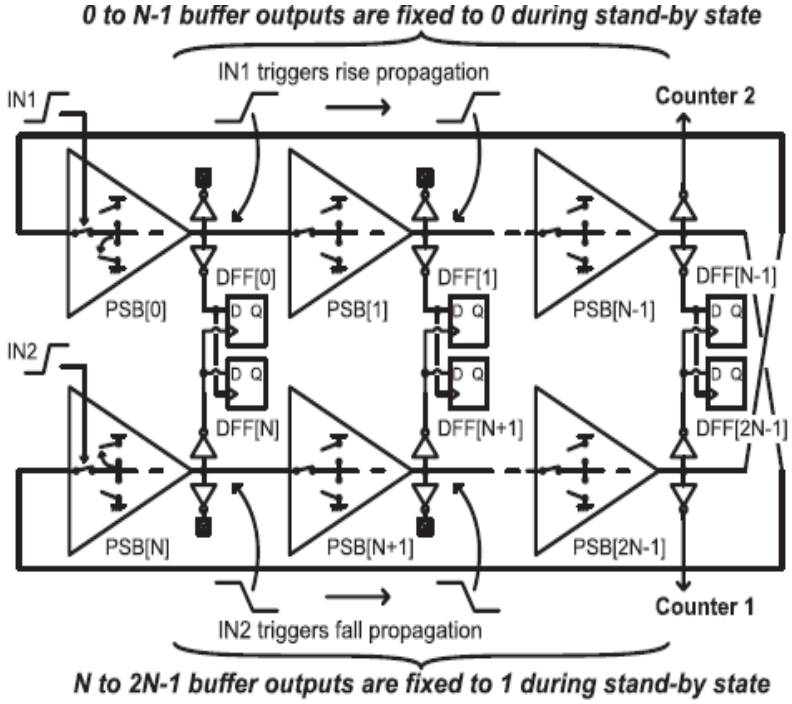


Figure no 5: Block diagram of the proposed fine TDC based on the PSBR

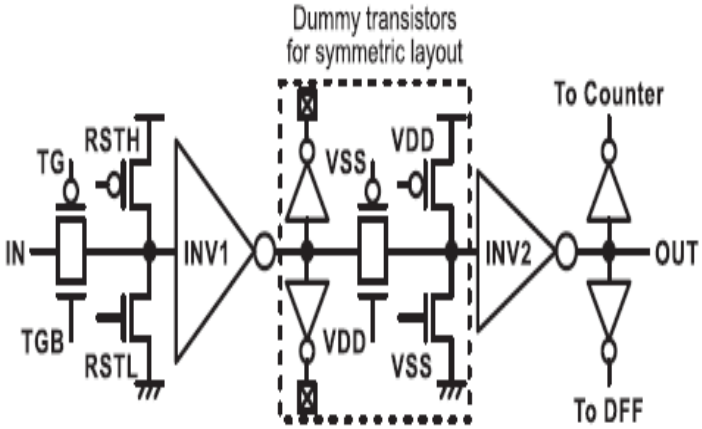


Figure no 6: Detailed schematic of the PSB

The remainder of this essay will be arranged as follows. The proposed TDC's design and conversion concept are described in Section II. The proposed TDC circuit implementation and post-layout simulation results are presented in Section III. The research comes to a conclusion in Section IV.

II. Proposed TDC Architecture in Two Steps

Pulse-Shrinking TDC Fine-Stage:

The PS buffering (PSBR)-based block diagram of the fine-stage TDC is shown in Figure 5. These components make up the majority of PS buffers with 2N stages (PSBs). On the other side of the ring, the (N + k) Th PSB output is linked to both the (N + k) Th and Kth DFF data inputs, and the Kth PSB output (k = 0, N 1) is connected to both the Kth DFF data input and the (N + k) Th DFF clock input. The PSBR's (N-1) and (2N-1) outputs are also connected to counters outside of the PSBR's core.

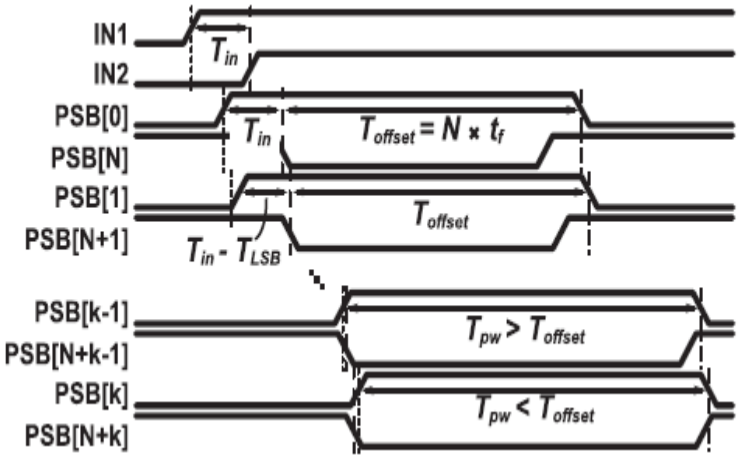


Figure no 7: Timing diagram of the PS TDC

The Kth PSB output rises later than the falling edge of the (N + k)this output, and the Kth DFF switches its output from 0 to 1 as the propagating pulse width T pw equals the initial built-in offset pulse width Offset, as shown in Fig. 8. By generating this DFF output transition, this TDC detects the first built-in Offset and triggers the completion warning. As a result, although T offset varies owing to technique variations, Offset's absolute value has no effect on the conversion process. The non-uniform shrinkage rate issue would have no effect on the proposed TDC since T offset is chosen by default to meet Offset>Th in Fig. 3.

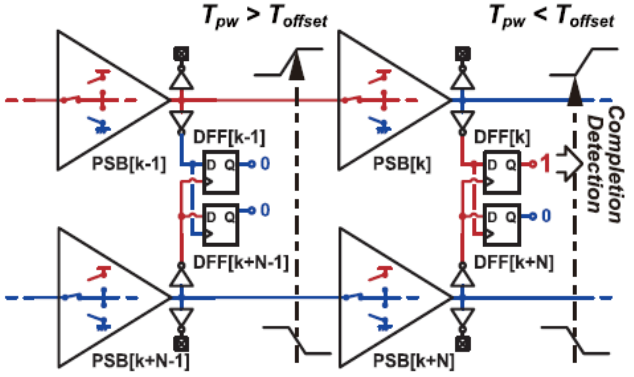


Figure no 8: Detailed PSBR schematic at the moment of the completion of conversion

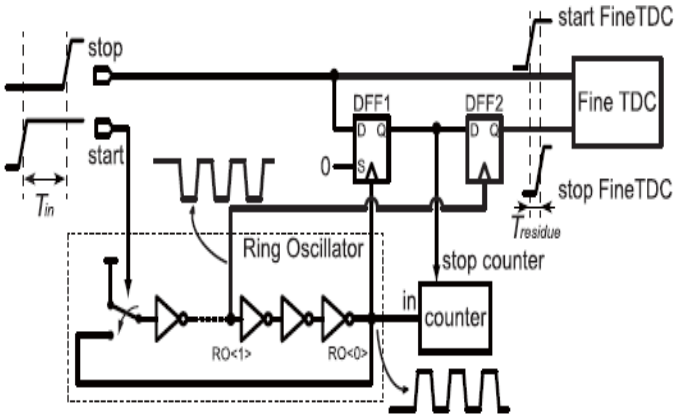


Figure no 9: Block diagram of the proposed TS TDC

Architecture of the Two-Step TDC:

Figure 9 depicts the proposed TS TDC design as a block diagram. A counter is included in a ring oscillator.

In Section II-A, the PS TDC serves as the coarse TDC, while the PS TDC serves as the fine stage. Unlike conventional TS TDCs, the suggested TDC connects the two TDCs with two DFFs to prevent the inter-stage multiplexers from becoming non-ideal. Although the fine TDC-linked second DFF, DFF2, in Fig. 9, seems to be unnecessary, it addresses a major stability issue in DFF1 caused by asynchronous time between RO0 and the input stop signal. The two DFFs are also used in the built-in tuning process outlined in Section II-C.

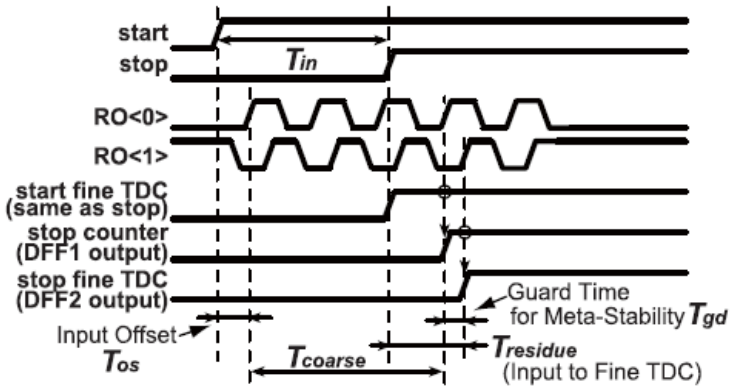


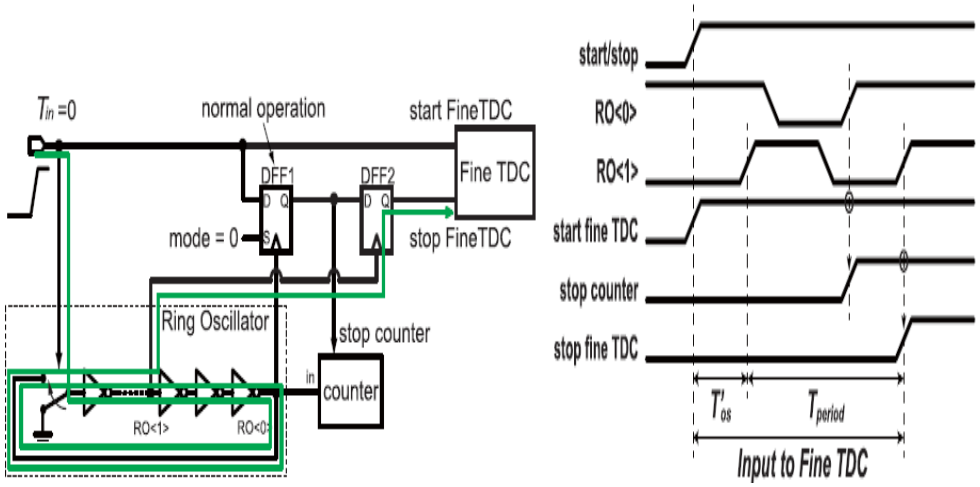
Figure no 10: Timing diagram of the proposed TS TDC

It functions as a timer to maintain met stability. Using the above-mentioned method, the period residue generated by this roundup, Residue, is injected for fine transfer into the second stage TDC. Finally, the total input time period is computed using the formula below:

$$T_{\text{in}} = T_{\text{os}} + T_{\text{coarse}} + T_{\text{gd}} - T_{\text{residue}}$$

Built-In Coarse Gain Calibration:

The optimum calibration technique is determined using the device's built-in calculating procedure. To calculate the required resolution ratio, divide the time interval corresponding to 1 LSB of the coarse TDC by the time interval corresponding to 1 LSB of the fine TDC. During the calibration phase, two alternative routes are switched using DFF1's S (Fixed) data, which is utilized to set its output Q to large, as shown in Figures 11 and 12. First and foremost, the first-stage inverter's input is set to GND until the calibration mode starts. When DFF1 is in regular mode with a 0 input to the S-port, as illustrated in Fig. 11, the fine TDC is halted after one coarse oscillation period plus the input offset time T, as shown in the timing diagram. (a).



(a) (b)

III. Prototype Implementation and Simulation

The proposed TS TDC is built in 0.18-m normal CMOS technology, as illustrated in Fig. Thirteen, and its, and are verified using post-layout emulation.

A kind of TDC is TDC Fine-Stage A.

The PSB placement in the fine TDC of the PSBR core, which comprises 32 PSB phases, is shown in the bottom part of Fig. 13. The Kth PSBs (k = 0,..., 15) and (k + 16) are positioned such that inter-PSB connection wire lengths are identical to relax the DFF relations illustrated in Fig. 5. Because of the importance of identifying the impact of jitter accumulation and manufacturing variation, the transistor size and current consumption of PSB inverters must be carefully chosen. Using eel's jitter study, the transistor sizes for the PSB were determined.

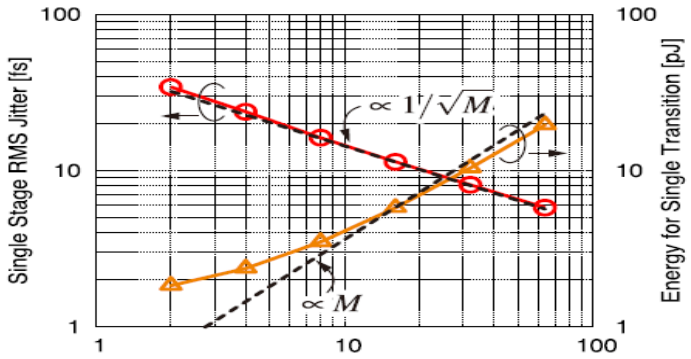


Figure no 11: Multiplier (m)

Improve schematic-level modeling with a single-stage PSB jitter and energy for a single increase transformation based on transistor width (Fig. Fig. Oh. 14). In PSB for INV1, Wombs = 8.32 = M am and Winos = 4.00 = M am. For INV2, Wombs = 8.00 M am and Winos = 4.00 M am. 1024 Monte Carlo runs of thermal noise simulations were used to determine the rams jitter. The jitter, or initial noise on the output capacitor, is caused by the white noise produced by the channel's resistance [17].

$$\sigma_{t_{dP}} \approx \sqrt{\frac{4kT\gamma_P t_{dP}}{I_P(V_{DD} - V_{tP})}}$$

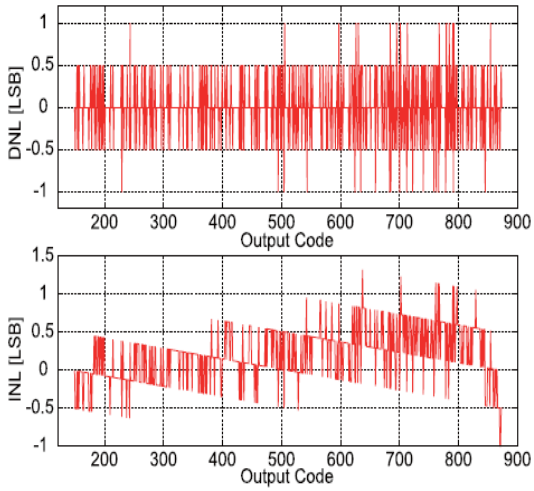


Figure no 12: Simulation results of DNL and INL of the fine-stage PS TDC

Two-Step TDC:

The jitter analysis from [17] is used to estimate transistor sizes in the coarse TDC ring oscillator, which includes 15 inverter stages. By sweeping the transistor distance, we utilized schematic-level simulation to validate the patterns of jitter and energy for a single increase transformation for the coarse stage ring oscillator, as shown in Fig. 17. The black dotted lines are normalized when the simulation effects are set at M = 16. Because the coarse staggering oscillator uses simple inverters, jitter and energy are clearly related to 1/M and M, respectively. Because the coarse stage in our TS TDC can cover a spectrum of up to 7 bits, and the limit is set at 7 bits, it can cover a spectrum of up to 7 bits.

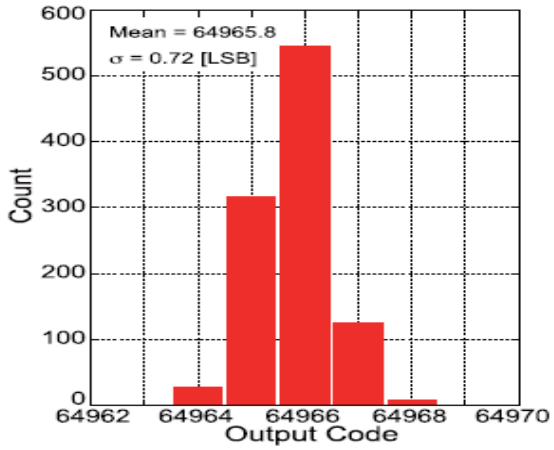


Figure no 13: Post-layout simulation result of single-shot code distribution of the TS TDC

Finish the conversion. The fine stage absorbs 47.8% of the total power in this instance, while the coarse stage absorbs the remainder. Figure 19 depicts a simulated DNL and INL. 19. 19. 19. The simulation range is in the middle of the input time interval range when the INL reaches its maximum, due to the slightly irregular shape produced by the calibration imperfection of the transfer characteristic of the TDC. The full transition function of this spectrum may be seen in Fig. Eighteen. The TDC's DNL and INL were respectively 1.0/+1.0 LSB and 2.0/+1.0 LSB.

Table no 1: compares the proposed TS TDC's efficiency to that of other previously reported sub-gate-delay resolution TDCs. To establish a fair comparison, the figure of merit (Form), which is widely used for TDC comparison, is employed

Ref.	TCAS'14 [6]	JSSC'10 [7]	MEJ'15 [9]	JSSC'12 [18]	JSSC'13 [19]	JSSC'14 [20]	ASSCC'16 [11]	This work
Architecture	3D Vernier	2D Vernier	Vernier Sub-Ranging	Cyclic	Two-Step (Time Amp.)	Pipeline	Pulse Shrinking (PS)	Two-Step PS
Tech. [nm] (Meas. / Sim.)	130 Meas.	65 Meas.	130 Meas.	130 Meas.	65 Meas.	65 Meas.	180 Meas.	180 Sim.**
Resol. [ps]	7	4.8	5	1.25	3.75	1.12	1.8	2.00
Precision rms [ps] (T_{in} at the meas. or sim.)	20.8 (@1.4 ns)	-	2.05 (0∼300 ps)	∼1.25* (@40 ps)	-	0.77 (@∼348 ps*)	2.16 (@860 ps)	1.44 (@129.5 ns)
Rate [MS/s]	25	50	20	50	200	250	4.4	3.3
Range [bit]	11	7	6	8	7	9	9	16
DNL [LSB]	0.8	1	0.63	0.7	0.9	0.6	1.2	1.5
INL [LSB]	1.5	3.3	1.47	3.0	2.3	1.7	8.7	4.2
Power [mW]	0.33(@1MHz)	1.7	1.15	4.3	3.6	15.4	3.4	18.0
Area [mm^2]	0.28	0.02	0.7	0.07	0.02	0.14	0.07	0.08
FoM [pJ/conv.-step]	0.40	1.14	1.96	1.34	0.46	0.32	14.6	0.43

* calculated from the figure of the measurement result. ** Monte-Carlo simulation result that leads to the worst FoM.

[6], [19], and [20] are now in use. As a consequence, the Type has gained widespread recognition.

$$\text{FoM} = \frac{\text{Power}}{(2^{N_{\text{linear}}} \times f_s)}$$

Where the effective number of linear bits (Linear) is given by

$$N_{\text{linear}} = \text{Range [bit]} - \log_2(\text{INL} + 1)$$

The Monte Carlo simulation results for the worst case M of the proposed TDC are shown. The proposed TDC, which is based on current 0.18-m CMOS technology, provides ultra-wide range and accurate time resolution at the same time, resulting in a competitive Form.

IV. Conclusion

This page discusses a variety of inputs as well as fine-time resolution mixing methods such as PS and TS. Traditional PS TDCs use a unique pulse injection with a built-in offset pulse and an offset pulse width detecting system to avoid an undesired non-uniformity of pulse shrinkage rate in the fine-stage PS TDC. As a consequence, fine resolution and low-jitter time-to-digital transmission are achieved, as well as the benefits of the PS TDC system, such as small-area deployment. To broaden the input spectrum, the proposed TS design is added to the PS TDC. The suggested TS TDC, which incorporates a built-in coarse gain calibration mechanism, addresses the functional problem caused by the non-ideality of inter-stage signal propagation direction and the gain difference between the two levels. The simulation revealed that the proposed TDC could simultaneously offer 16-bit broad dynamic range and 2.0-ps fine resolution. It is feasible to get a From that is competitive. This TDC features a sub-gate-delay resolution and mature 0.18-m technology, unlike previously reported TDCs with sub-gate-delay resolution and mature 0.18-m technology.

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